SSI2100

PROCIRCUIT™ 512-STAGE BUCKET BRIGADE DELAY*

The SSI2100 is a new generation bucket brigade delay, developed on a modern IC process for performance improvements and new features while preserving the "mojo" of such beloved and quirky analog delay circuits.

A 512-stage bucket chain allows a wide range of delay times from a clock frequency of 1kHz to over 2MHz.

A novel circuit (patent pending) allows easy connection of multiple SSI2100's for longer delay times without having to recalibrate inputs and outputs. An additional benefit to daisy-chaining is access to intermediate feedback taps for interesting reverb and other psychoacoustic effects.

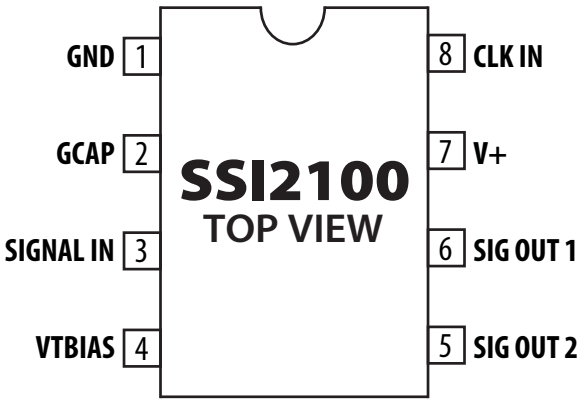
An integrated clock driver greatly simplifies external clock sourcing and is TTL-compatible, making a companion BBD clock IC unnecesary.

Also on-chip is a tetrode bias voltage generator that eliminates the need for externally providing the legacy "14/15 V_{GG}" supply voltage.

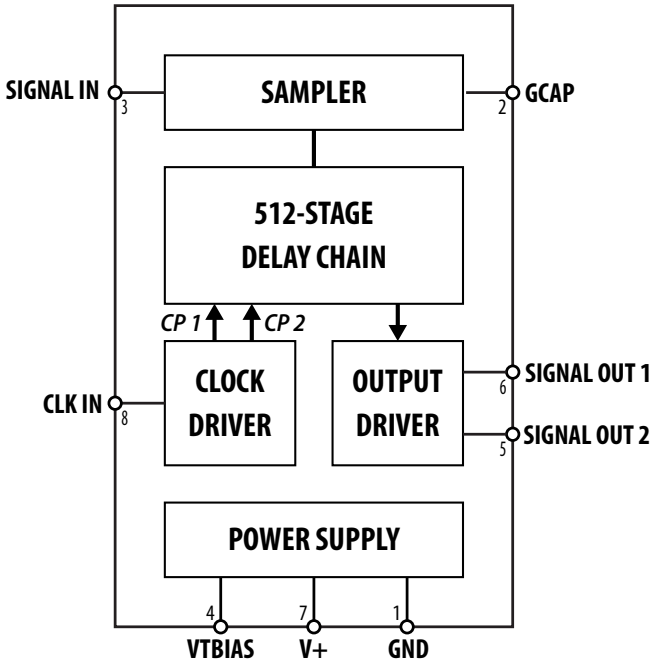
The SSI2100 is available in a super-compact 8-lead SOP surface-mount package.

FEATURES

- **First Modern BBD Design in Decades**
- **512-Stage Delay Chain With Clock Range from 1kHz to over 2MHz**
- **Easy Daisy-Chaining of Multiple Units for Longer Delays and Access to Intermediate Taps**
- **On-Chip Clock Driver with TTL/CMOS 5V and 3.3V Compatible Input**
- **Compact SOP8 Surface-Mount Package**
- **Single 5V Operation**



PIN CONNECTIONS
8-LEAD SOP



FUNCTIONAL BLOCK DIAGRAM

*Patent Pending

The SSI2100 is available exclusively from Sound Semiconductor and its authorized resellers
PO Box 1587, Arroyo Grande, CA 93421 USA, www.soundsemiconductor.com
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SPECIFICATIONS (V+ = 5.0V, GCAP = GND, f_{CLK} = 40kHz, V_{IN} = 0.2V_{P-P}, F_{IN} = 1kHz, T_A = 25°C; using Figure 1 circuit)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
Supply Voltage Range	V+		4.75	5.0	5.25	V
Supply Current	I+			0.4	0.6	mA
Tetrode Bias Voltage Range	V_{TBIAS}		4.55	4.65	4.75	V
SIGNAL INPUT						
Frequency Range		Output 3dB down	15			kHz
Optimal Input Signal Range		THD = <1%	40		440	mV_{PP}
Insertion Loss			-1.2	-1.6	-2.0	dB
DC Bias Voltage		at Pin 3		3.20		V
SIGNAL OUTPUT						
Output Offset Voltage				2.4		V
Signal Path Gain		GCAP = GND		2.0		dB
		GCAP = V+		6.0		dB
CLOCK DRIVER INPUT						
Operating Frequency	F_{CLK}		1		2000	kHz
Logic Clock H Level	V_{IH}		2.5			V
Logic Clock L Level	V_{IL}				1.5	V
Logic Clock Rise/Fall Time	t_R, t_F				100	ns
Duty Cycle				50		%
Input Capacitance				5		pF
PERFORMANCE						
Output Noise Voltage		V_{IN} = GND, A-Weighted		0.14		mV_{RMS}
Signal-to-Noise Ratio	SNR	A-Weighted, at 1% THD		61		dB
Total Harmonic Distortion	THD	V_{IN} = 70mV_{RMS}		0.22		%

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7V
Maximum Voltage into Pins	7V
Maximum Output Voltage	7V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Lead Temperature (Soldering, 10 sec)	260°C

ORDERING INFORMATION

Part Number	Package Type/Container	Quantity
SSI2100S-TU	8-Lead SOP* - Tube	100
SSI2100S-RT	8-Lead SOP* - Tape and Reel	4000

*SSI Package ID "**PSL8**", compliant with JEDEC MS-012-AA
Mechanical drawing available at www.soundsemiconductor.com

PIN DESCRIPTIONS

Pin(s)	Name	Description
1	GND	Connect to analog signal ground with short, low inductance trace.
2	GCAP	Gain Capacitor Enable. Tie to GND for low gain, and to V+ for high gain.
3	SIGNAL IN	Audio signal input. Requires a DC bias of 3.20V for correct operation, and a low-impedance source to drive the internal sample-and-hold.
4	VTBIAS	Internally-generated 14/15 of V+. Connect a 3.3µF capacitor to GND.
5	SIG OUT 2	Output when CLK IN is high. Source follower.
6	SIG OUT 1	Output when CLK IN is low. Source follower.
7	V+	+5V supply. Recommend 100nF local decoupling capacitor placed as close to package as possible with a low inductance trace to ground.
8	CLK IN	Clock input to internal clock generator, producing two anti-phase buffered clock signals for the delay chain. Compatible with both 3.3V and 5V logic thresholds.

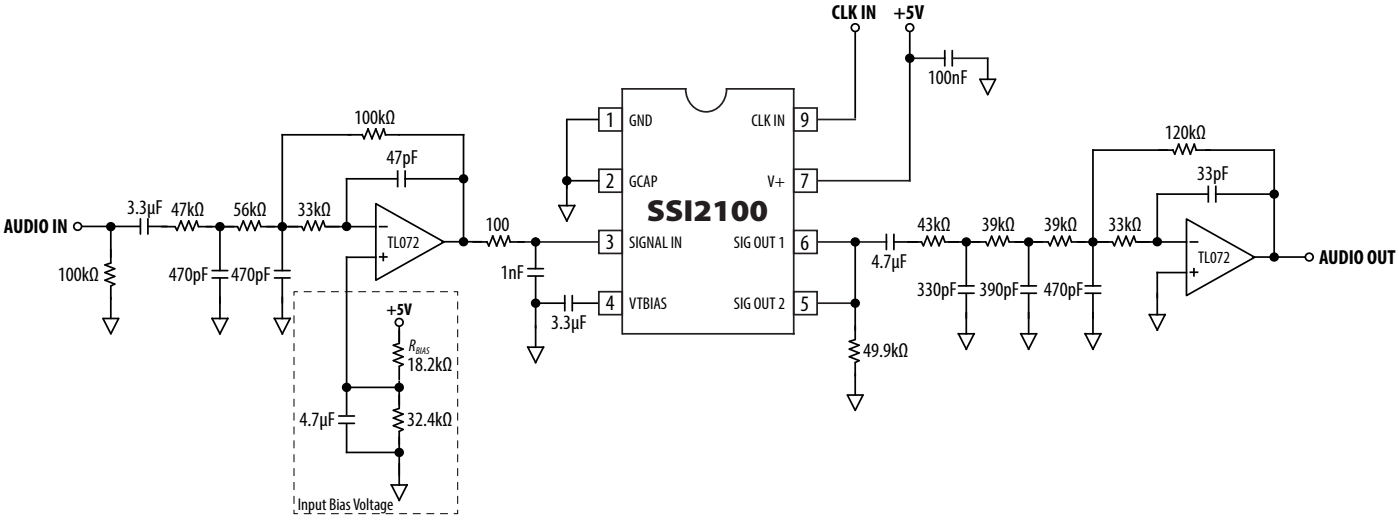

Figure 1: Typical Application Circuit
Input and output filters are set to 15kHz cut-off frequencies.

USING THE SSI2100

The SSI2100 is a new generation CMOS bucket brigade delay (BBD). It comprises a sample-and-hold with programmable storage capacitor, a 512-stage switched capacitor delay line, a two-stage output driver, internal clock driver and clock tree, and internal V_{TBIAS} network.

Typical Application

Figure 1 shows a typical application circuit. BBDs are sampled data devices so the first circuit block is an anti-aliasing filter on the input to remove any signal frequencies above half the clock frequency. The filter as shown is a 3-pole low-pass filter with AC-coupled input, and the DC bias applied to the filter as well. The filter output couples to the input of the SSI2100 through an RC network to stabilize the signal during sampling windows. In this example the gain setting pin GCAP is connected to ground to give a signal path gain of close to 0dB.

The output of the SSI2100 is a train of pulses from the two source-follower outputs. The outputs are combined into a common load resistor, and then AC-coupled into a 4-pole low-pass reconstruction filter, again set to half the clock frequency.

The internal V_{TBIAS} network needs an external 3.3µF capacitor connected from pin 4 to ground.

The SSI2100 requires a single TTL/CMOS-compatible square-wave clock signal to drive the internal clock tree.

Power Supply and Grounding

The SSI2100 is a 5V-only device. The positive supply V+ must be fed from a regulated 5V source. It should have a local 100nF good quality ceramic decoupling capacitor placed close to the supply pin, together with local bulk supply rail decoupling capacitors of 10µF or more, and with good ground and supply trace routing practices applied throughout.

The SSI2100 has one ground connection on pin 1. It must be connected to ground using thick short traces or closely positioned vias to a ground plane.

Signal Input

The signal input (pin 3) to the SSI2100 looks like a sample-and-hold operating at the clock frequency. When the clock signal is low the sampling switch is open and connects the signal source to the internal sampling capacitor. The sampling capacitor is between 5pF and 10pF depending on ther gain setting (see below).

Under certain signal conditions a considerable short pulse of current can occur at the start of the sampling period. It is recommended that an external 1nF capacitor and series 100Ω resistor are used to isolate op amp outputs from this dynamic load, which could otherwise cause the op amp to ring at each sample point.

The maximum signal range of the input is 440mV peak-to-peak. The low noise floor of the SSI2100 allows for a wide dynamic range at the input. The signal input also needs a DC bias of 3.20V – there are several ways to achieve this; the circuit in Figure 1 applies the bias as an offset to the input filter. Care should be taken in the design of the bias system to ensure it has a low impedance.

BBDs are inherently sampled-data systems. As such the applied signal must meet the Nyquist criterion of no frequency components greater than the clock frequency; otherwise they will alias down into the audio band and introduce unwanted distortion. To prevent this it is recommended to use an anti-alias filter, such as shown in Figure 1. For applications with variable clock frequencies you can either implement a sweepable filter to track the clock frequency, or use a fixed filter set to the highest frequency of interest and then ensure that the minimum clock frequency is at least twice that.

Gain Control (GCAP)

The gain capacitor selection input (pin 2) enables and disables an additional capacitor in the sample-and-hold circuit. Due to the way BBDs operate this has the effect of applying additional gain to the signal at the front of the BBD for applications that may require it, such as chaining (discussed later).

The GCAP pin must be tied either to GND for standard gain, or to V+ for high gain. It must not be left floating.

Signal Outputs

The SSI2100 has two antiphase outputs from the BBD chain. Each output is a source-follower from an internal n-channel MOSFET. External circuits must provide a load to the outputs, either individually or commoned. Outputs may be used independently as well, such as when chaining.

Both outputs contain considerable clock energy which must be removed using a reconstruction filter. This filter has the same Nyquist frequency requirement of the input filter. The output filter shown in Figure 1 is a 4-pole low-pass filter with AC-coupled input to remove the DC output bias.

Output Trimming

The two output pins provide anti-phase outputs. Due to variation in the output transistors there may be small differences in the two output levels, which appears as a low-level injection of the clock signal. To compensate for this an alternative output circuit using a trimmer can be used as shown in Figure 2.

In applications where the clock signal is sufficiently high enough and the reconstruction filter transition band is steep enough the trim circuit may not be required.

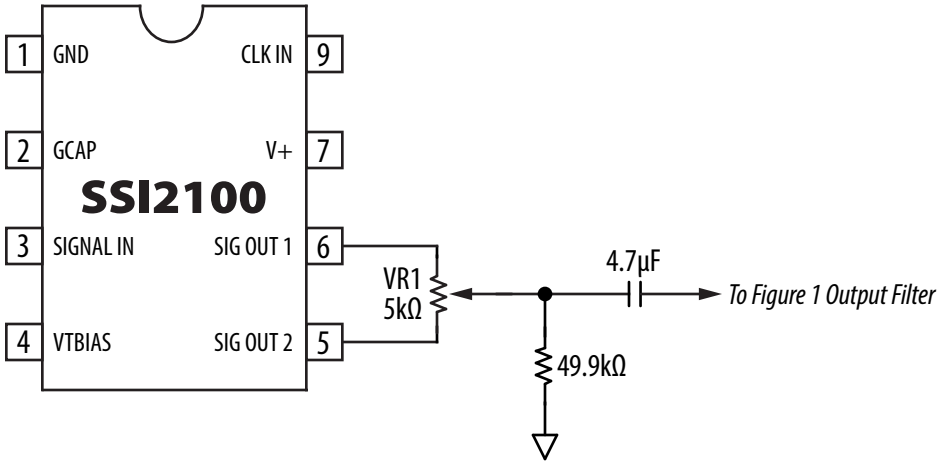

Figure 2: Optional Output Symmetry Trim

Trimming the output can be either by ear or by measurement (e.g., oscilloscope or audio analyser). Start with the trimmer at one end of the track and move the trimmer until the minimum clock noise point is found (you might need to move back and forth to find the best trim point). Once set it is recommended to lock the trimmer with a drop of paint or similar (nail varnish is rather good at this).

Clocking

The clock input (pin 8) is compatible with TTL and CMOS logic levels in both 5V and 3.3V systems. It should be driven by a square wave with equal high and low periods and fast transitions. If your design cannot guarantee this requirement then we recommend using a flip-flop to ensure a clean square wave, and then to double the frequency range of the clock source to compensate.

The clock frequency range of the SSI2100 is very wide, and will perform within specifications from 1 kHz to over 2MHz. It can be clocked both lower and higher with some degradation in performance. As the SSI2100 is a sample-based device its behavior is subject to Nyquist limits, where the clock signal needs to be at least twice the highest signal present in the input signal.

Tetrode Bias (V_{TBIAS})

The SSI2100 has an internal V_{TBIAS} generator. For normal operation it requires a 3.3µF capacitor connected from pin 4 to ground. This voltage (sometimes called V_{GG}) is used to bias the internal tetrode transistors in the delay chain to improve performance. Refer to the Principles of Operation section for a description of the tetrode transistors.

Critical Component Selection

There are very few critical components for the SSI2100.

The supply decoupling capacitor should be a good quality 100nF ceramic capacitor of at least X7R dielectric. It should be placed as close to the supply pin as possible, with a low-impedance trace to a ground.

The V_{TBIAS} capacitor should be a good quality electrolytic. For very high clock frequencies it is recommended to connect a smaller value capacitor (e.g., 100nF ceramic X7R) in parallel to reduce impedance of the bypass capacitance.

–ADDITIONAL CONTENT COMING SOON!–